REMARKS

In response to the Office Action mailed February 6, 2008, Applicants respectfully request reconsideration. Each of the issues raised in the Office Action is addressed herein.

Claims 1-7 are pending in this application, of which claims 1 and 5 are independent claims. In this amendment, claims 1 and 5 have been amended. No new matter has been added. The application as now presented is believe to be in allowable condition.

Summary of Telephone Conference with Examiner

Applicants' representative Joseph Teja and Technology Specialist Daniel Wehner appreciate the courtesies extended by Examiner Jesse Moll in granting and conducting a telephone conference on May 5, 2008.

During the telephone conference, independent claims 1 and 5 were discussed with respect to rejections of the claims over the cited Cheon reference (U.S. Patent No. 6,070,210). Applicants' representative explained that Cheon does not appear to disclose or suggest the last limitation of claim 1, "processing the first digital messages and the at least one second digital message via the analysis tool to analyze operation of the microprocessor and the at least one second specific event." The Examiner provided his characterization of the Cheon reference, as set forth in further detail below.

Claim 5 was also briefly discussed, and the Examiner indicated that he was considering the memory integrated with the microprocessor recited in claim 5 to be inherent to the microprocessor of Cheon.

Further details of the telephone conference are set forth below.

Rejections Under 35 U.S.C. §102

Claims 1-7 were rejected under 35 U.S.C. 102(b) as being allegedly anticipated by U.S. Patent No. 6,070,210 (hereafter, "Cheon"). Applicants respectfully traverse these rejections to the extent that they are maintained over the claims as amended herein.

In connection with claim 1, the Office Action contends that Cheon allegedly discloses an analysis tool, referring to the memory 110 shown in Cheon's Fig. 2 (Office Action, page 3) and asserts that "inherently, if the messages are received to memory 110, they must be processed,"

and that "any message is related to and is intended to analyze some portion of processor operation." During the telephone conference, the Examiner asserted that the terms "processing" and "analyze operation of the microprocessor," as recited in the last limitation of claim 1, were broad enough to encompass processing an instruction to store data in the memory 110 and thereby determining (i.e., analyzing) that the microprocessor sent a message to store data on the memory 110, and that Cheon's disclosure in connection with the memory 110 therefore taught the "processing" and "analyzing" limitations of claim 1. Applicants respectfully disagree with this characterization.

While Applicants do not accede to the propriety of the rejection based on such a characterization, each of claims 1 and 5 has been amended nonetheless to indicate that analyzing the operation of the microprocessor by the analysis tool includes determining the instruction sequence executed by the microprocessor.

Thus, as amended, independent claim 1 recites a method comprising transmitting first digital messages to an analysis tool from a monitoring circuit integrated with a microprocessor. The first digital messages are representative of first specific events which depend on execution of an instruction sequence by the microprocessor. The method further comprises detecting, with a request circuit, at least one second specific event independent from the execution of the instruction sequence by the microprocessor, and transmitting to the monitoring circuit, when the at least one second specific event is detected, a characteristic data signal associated with said at least one second specific event. The method further comprises storing the characteristic data signal in the monitoring circuit and, if resource management conditions are fulfilled, transmitting an acknowledgement signal to the request circuit. The method further comprises transmitting at least one second digital message representative of the stored characteristic data signal to the analysis tool, and processing the first digital messages and the at least one second digital message via the analysis tool to analyze operation of the microprocessor, **including determining the instruction sequence executed by the microprocessor**, and the at least one second specific event.

Claim 5 is an independent apparatus claim that closely tracks the language of independent method claim 1. As amended, claim 5 recites an apparatus comprising a microprocessor, a memory integrated with the microprocessor, an analysis tool, and a monitoring

circuit for transmitting first digital messages to the analysis tool. The first digital messages are representative of first specific events which depend on execution of an instruction sequence by the microprocessor. The apparatus further comprises a request circuit for detecting at least one second specific event independent from the execution of the instruction sequence by the microprocessor. The request circuit transmits to the monitoring circuit, when the at least one second specific event is detected, a request signal and a characteristic data signal associated with said at least one second specific event. The monitoring circuit stores the characteristic data signal, transmits to the request circuit an acknowledgement signal when the characteristic data signal is stored, and transmits to the analysis tool at least one second digital message representative of said stored characteristic data signal. The analysis tool processes the first digital messages and the at least one second digital message to analyze operation of the microprocessor, **including determining the instruction sequence executed by the microprocessor**, and the at least one second specific event.

Cheon fails to disclose or suggest all of the elements of independent claims 1 and 5, respectively. For example, Cheon fails to disclose or suggest processing first digital messages and at least one second digital message, via an analysis tool, to analyze operation of a microprocessor, **including determining the instruction sequence executed by the microprocessor**, and at least one second specific event.

In Cheon, a microprocessor sends a "low" state or "high" state mode selection control signal to buffers 210 and 220 in circuitry associated with the DMA device to enable or disable acknowledgement signals DACK and BACK transferred between the SCSI controller and the DMA device. The state of the mode selection control signal, and thus which acknowledgement signal is active, determines the timing mode (i.e., single vs. burst mode) used to transfer data from the DMA device to the memory (Cheon, Fig. 2 and accompanying text at col. 3, line 65 – col. 4 line 26). Clearly this single control signal sent by the microprocessor of Cheon to change the timing mode of data transfer cannot be used by the memory to determine an instruction sequence executed by the microprocessor, as recited in each of amended independent claims 1 and 5.

For at least the foregoing reasons, each of claims 1 and 5 patentably distinguishes over Cheon and is in condition for allowance. Therefore, the rejections of claims 1 and 5 under 35 U.S.C. 102(b) as being anticipated by Cheon should be withdrawn.

Claims 2-4 and 6-7 depend from one of claims 1 and 5 and are allowable based at least upon their dependency.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: May 6, 2008

Respectfully submitted,

By: _____

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